## **CLAIMS**

## What is claimed is:

1	1	Λn	annaratue	comprising:
1	1	. An	apparatus	compusing.

- a plurality of strobe inputs to receive a plurality of strobe signals;
- a plurality of data inputs to receive a plurality of data signals transmitted in
- a transaction in conjunction with said plurality of strobe signals in a
- 5 source synchronous manner;
- bus control logic to produce an externally visible indication that an error
- has occurred if a glitch on one or more of said plurality of strobe
- 8 signals is detected.
- 2. The apparatus of claim 1 wherein said bus control logic is to produce the externally
- 2 visible indication that the error has occurred by retrying the transaction.
- 1 3. The apparatus of claim 1 wherein said bus control logic is to disregard data signals
- 2 latched in conjunction with said glitch.
- 4. The apparatus of claim 3 wherein said bus control logic is to initiate said
- 2 transaction by requesting a data item, and wherein said bus control logic is further to
- 3 initiate a second transaction to retrieve said data item in response to said glitch being

- 4 detected.
- 5. The apparatus of claim 2 wherein said bus control logic is also, in response said
- error, to stop sending additional bus requests, and to disregard data received in
- 3 conjunction with said transaction.
- 6. The apparatus of claim 5 wherein said bus controller is to retry said transaction
- 2 after waiting until no further strobes are outstanding.
- 1 7. A bus agent comprising:
- a plurality of data signal inputs to receive a plurality of data signals;
- a plurality of strobe inputs to receive a plurality of strobe signals;
- a state machine coupled to receive said plurality of strobe signals and to
- 5 generate therefrom a plurality of clock signals;
- a strobe glitch detection circuit to monitor said plurality of clock signals
- produced by said state machine to detect glitches on one or more of
- 8 said plurality of strobe signals.
- 1 8. The bus agent of claim 7 wherein said state machine is to receive two
- 2 complementary strobe signals and to generate therefrom four non-overlapping clock
- 3 signals, said four non-overlapping clock signals having sequential active periods, and

- 4 wherein said strobe glitch detection circuit is coupled to receive two clock signals of
- said four non-overlapping clock signals, and further wherein said strobe glitch
- 6 detection circuit is to generate an error signal if a first one of said two clock signals is
- 7 in an incorrect state at a time determined from the other one of said two clock signals.
- 9. The bus agent of claim 8 wherein said strobe glitch detection circuit is to generate
- 2 the error signal if the first one of said two clock signals is in the incorrect state after a
- 3 delay duration.
- 1 10. The bus agent of claim 9 wherein said four non-overlapping clocks have a
- 2 substantially similar active period, and wherein said delay duration is less than a
- 3 duration of said active period.
- 1 11. The bus agent of claim 7 wherein said plurality of strobe signals is a first set of a
- 2 first number of strobe signals and wherein said plurality of clocks are a second set of a
- 3 second number of clocks, said second number being twice the first number, said
- 4 plurality of clocks being non-overlapping clocks.
- 1 12. The bus agent of claim 7 wherein said plurality of data signals comprise a
- 2 plurality of sets of data signals, each set having an associated strobe and an inverted
- 3 strobe signal, and wherein said strobe glitch detection circuit comprises a plurality of

- 4 strobe glitch detectors, each of said plurality of strobe glitch detectors being coupled to
- 5 receive a first clock signal and a second clock signal from said plurality of clock
- 6 signals and to generate a glitch indicator signal if said second clock signal is in an
- 7 incorrect state after a predetermined duration measured from a transition of the first
- 8 clock signal.
- 13. The bus agent of claim 12 wherein each glitch detector comprises:
- a delay circuit to receive said first clock signal and to generate a delayed
- 3 first clock signal;
- a latch clocked by said delayed first clock signal, said latch being a falling
- edge clock triggered latch, said latch having a data input coupled to
- receive said second clock signal and to generate an output error signal
- if said second clock signal is absent when a falling edge of the delayed
- 8 first clock signal clocks the latch.
- 1 14. The bus agent of claim 13 wherein said output error signal is further coupled to
- 2 said latch to retain the output error signal in an active state until a reset signal is
- 3 received.
- 1 15. The bus agent of claim 14 further comprising:
- a bus controller to retry a transaction during which a strobe glitch is

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being detected.

3	detected in response to detection of said strobe glitch.
1	16. The bus agent of claim 15 wherein said bus controller is also, in response said
2	output error signal, to stop sending additional bus requests, to disregard data received
3	in conjunction with said transaction, and to reset each glitch detector.
1 2	17. The bus agent of claim 16 wherein said bus controller is to reset each glitch when no further strobes are outstanding.
1	18. The bus agent of claim 7 further comprising:
2	a bus controller to retry a transaction during which a glitch is detected by
3	said strobe glitch detection circuit.
1	19. A system comprising:
2	a first bus agent capable of generating data signals and accompanying
3	strobe signals for source synchronous transmission of at least a portion
4	of a transaction;
5	a second bus agent capable of detecting a glitch on said strobe signals, said
6	second bus agent retrying said transaction in response to the glitch

- 1 20. The system of claim 19 wherein said second bus agent is to disregard data signals
- 2 latched in conjunction with said glitch.
- 1 21. The system of claim 20 wherein said second bus agent is to retry said transaction
- 2 after waiting until no further strobes are pending.
- 1 22. The system of claim 19 wherein said second bus agent is to retry said request
- without signaling an error or requesting system restart.
- 1 23. A method comprising:
- 2 receiving a plurality of strobe signals;
- generating a plurality of internal clock signals from said plurality of strobe
- 4 signals;
- detecting one of said plurality of internal clock signals being in an incorrect
- state with respect to another one of said plurality of internal clock
- 7 signals.
- 1 24. The method of claim 23 further comprising:
- 2 producing an externally visible signal that an error has occurred.
- 1 25. The method of claim 24 wherein producing an externally visible signal that the

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- 23 error has occurred comprises retrying a data transfer during which the error occurred. 2 26. The method of claim 23 wherein detecting comprises: 1 delaying a first internal clock to produce a delayed first internal clock; 2 latching said second internal clock with said delayed first internal clock to 3 produce an error signal in response to said second internal clock being in the incorrect state when latched by said delayed first internal clock. 5 27. The method of claim 23 wherein said plurality of internal clock signals have 1 different duty cycles than said strobe signals. 2 28. A method comprising: 1 requesting data over a source synchronous bus; 2 receiving data and a plurality of strobe signals over said source 3 synchronous bus; 4 detecting a glitch in at least one of said plurality of strobe signals; and 5
  - 29. The method of claim 28 further comprising: 1
- waiting until no further strobes are pending to retry said transaction. 2

retrying a transaction to retrieve said data.

- 1 30. The method of claim 29 further comprising:
- disregarding any data latched in conjunction with said glitch.